

# NLA16T245

## 16-Bit (Dual 8-Bit) Configurable Dual-Supply Translating Transceiver with 3-State Outputs

The NLA16T245 is a 16-bit (dual 8-bit) configurable dual-supply translating bidirectional transceiver with 3-state outputs. The A- and B-ports are designed to track two different power supply rails,  $V_{CCA}$  and  $V_{CCB}$  respectively. Both supply rails are configurable from 0.9 V to 4.5 V allowing universal bidirectional voltage translation between the A- and B-ports.

The Direction inputs, 1DIR and 2DIR, determine the direction of data flow. 1DIR and 2DIR are independent of each other. When 1DIR or 2DIR is High, data flows from 1An to 1Bn or 2An to 2Bn respectively. When 1DIR or 2DIR is Low, data flows from 1Bn to 1An or 2Bn to 2An respectively. The Output Enable inputs, and , when High, disables both A- and B-ports by putting them in 3-state. The 1DIR, 2DIR, and signals are all designed to track  $V_{CCA}$ .

### Features

- Wide  $V_{CCA}$  and  $V_{CCB}$  Operating Range: 0.9 V to 4.5 V
- Output Noise Reduction through Dynamic Output Impedance Change
- Drive Capability:  $\pm 12$  mA @ 3.0 V  $V_{CC}$
- Input/Output Pins OVT to 5.5 V
- Control Inputs Track  $V_{CCA}$
- Non-preferential  $V_{CC}$  Sequencing
- Outputs at 3-State until Active  $V_{CC}$  is reached
- Power-Off Protection
- Outputs Switch to 3-State with either  $V_{CC}$  at GND
- Pb-Free Packaging: TSSOP-48
- This is a Pb-Free Device

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices

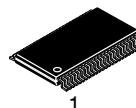
### Important Information

- ESD Protection for All Pins:  
Human Body Model (HBM) > 2000 V  
Machine Model (MM) > 200 V



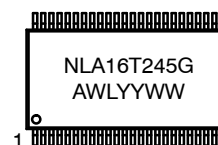
ON Semiconductor®

<http://onsemi.com>



TSSOP-48  
DT SUFFIX  
CASE1201

### MARKING DIAGRAM



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NLA16T245DTR2G	TSSOP-48 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NLA16T245

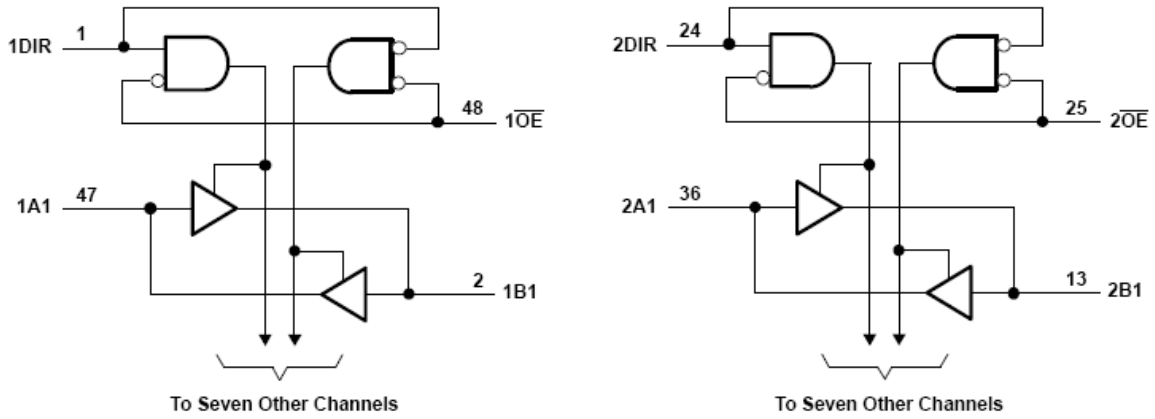


Figure 1. Logic Diagram

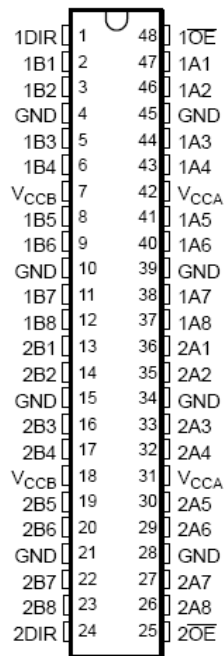


Figure 2. Pin Assignment

### Pin Names

Pins	Description
V <sub>CCA</sub>	A-Port DC Power Supply
V <sub>CCB</sub>	B-Port DC Power Supply
GND	Ground
$\overline{1OE}$ , $\overline{2OE}$	Output Enable Pins
1DIR, 2DIR	Direction Select Pins
1A <sub>n</sub> , 2A <sub>n</sub>	A-Port I/O
1B <sub>n</sub> , 2B <sub>n</sub>	B-Port I/O

### Function table

$\overline{nOE}$	nDIR	Operating Mode
L	L	nB to nA
L	H	nA to nB
H	X	nA and nB Ports at Hi-Z

# NLA16T245

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CCA}, V_{CCB}$	DC Supply Voltage	-0.5 to +5.5		V
$V_I$	Input Voltage	$\overline{nOE}, nDIR, nA$ -0.5 to +4.6	$V_{CCA} = 0\text{ V}$	V
		-0.5 to +5.5	$V_{CCA} \geq 0.9\text{ V}$	
		$nB$ -0.5 to +4.6	$V_{CCB} = 0\text{ V}$	
		-0.5 to +5.5	$V_{CCB} \geq 0.9\text{ V}$	
$V_O$	Output Voltage	(Power-Off Mode) $nA, nB$ -0.5 to +5.5	$V_{CCA}$ or $V_{CCB} = 0$	V
		(3-State Mode) $nA, nB$ -0.5 to +5.5	$V_{CCA}, V_{CCB} \geq 0.9\text{ V}$	
		(Active Mode - High or Low State) $nA$ -0.5 to $V_{CCA} + 0.5$	$V_{CCA}, V_{CCB} \geq 0.9\text{ V}$	
		(Active Mode - High or Low State) $nB$ -0.5 to $V_{CCB} + 0.5$		
$I_{IK}$	DC Input Diode Current	$\overline{nOE}, nDIR$ -50	$V_I < \text{GND}$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +125		$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CCA}, V_{CCB}$	Positive DC Supply Voltage	0.9	4.5	V
$V_I$	Input Voltage	GND	4.5	V
$V_O$	Output Voltage	GND	4.5	V
	(Power Down) $nA, nB$			
	(3-State Mode) $nA, nB$	GND	4.5	
	(Active Mode - High or Low State) $nA$	GND	$V_{CCA}$	
	(Active Mode - High or Low State) $nB$	GND	$V_{CCB}$	
$T_A$	Operating Temperature Range	-55	+115	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Transition Rise or Rate $V_I, V_{IO}$ from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0	10	nS

# NLA16T245

## DC ELECTRICAL CHARACTERISTICS (INPUT)

Symbol	Parameter	Test Conditions	V <sub>CCI</sub> (Note 1) (V)	V <sub>CCO</sub> (Note 2) (V)	-55°C to +115°C		Unit
					Min	Max	
V <sub>IH</sub>	Input HIGH Voltage, Data Inputs		3.6 – 4.5	0.9 – 4.5	2.2		V
			2.7 – 3.6		2.0		
			1.95 – 2.7		1.7		
			1.2 – 1.95		0.65 * V <sub>CCI</sub>		
			0.9 – 1.2		0.9 * V <sub>CCI</sub>		
V <sub>IL</sub>	Input LOW Voltage, Data Inputs		3.6 – 4.5	0.9 – 4.5		0.8	V
			2.7 – 3.6			0.8	
			1.95 – 2.7			0.7	
			1.2 – 1.95			0.35 * V <sub>CCI</sub>	
			0.9 – 1.2			0.1 * V <sub>CCI</sub>	
V <sub>IH</sub>	Input HIGH Voltage, Control Inputs	Referenced to V <sub>CCA</sub>	3.6 – 4.5		2.2		V
			2.7 – 3.6		2.0		
			1.95 – 2.7		1.6		
			1.2 – 1.95		0.65 * V <sub>CCA</sub>		
			0.9 – 1.2		0.9 * V <sub>CCA</sub>		
V <sub>IL</sub>	Input LOW Voltage, Control Inputs	Referenced to V <sub>CCA</sub>	3.6 – 4.5			0.8	V
			2.7 – 3.6			0.8	
			1.95 – 2.7			0.7	
			1.2 – 1.95			0.35 * V <sub>CCA</sub>	
			0.9 – 1.2			0.1 * V <sub>CCA</sub>	

NOTE: Connect ground before applying supply voltage V<sub>CCA</sub> or V<sub>CCB</sub>. This device is designed with the feature that the power-up sequence of V<sub>CCA</sub> and V<sub>CCB</sub> will not damage the IC.

1. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
2. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

# NLA16T245

## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	V <sub>CCA</sub> (V)	V <sub>CCB</sub> (V)	-55°C to +115°C		Unit	
					Min	Max		
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA; V <sub>I</sub> = V <sub>IH</sub>	0.9 – 4.5	0.9 – 4.5	V <sub>CCO</sub> – 0.2		V	
		I <sub>OH</sub> = -0.5 mA; V <sub>I</sub> = V <sub>IH</sub>	0.9	0.9	0.75 * V <sub>CCO</sub>			
		I <sub>OH</sub> = -2 mA; V <sub>I</sub> = V <sub>IH</sub>	1.4	1.4	1.05			
		I <sub>OH</sub> = -4 mA; V <sub>I</sub> = V <sub>IH</sub>	1.65	1.65	1.2			
		I <sub>OH</sub> = -8 mA; V <sub>I</sub> = V <sub>IH</sub>	2.3	2.3	1.75			
		I <sub>OH</sub> = -12 mA; V <sub>I</sub> = V <sub>IH</sub>	3.0	3.0	2.3			
		I <sub>OH</sub> = -12 mA; V <sub>I</sub> = V <sub>IH</sub>	4.5	4.5	4.0			
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA; V <sub>I</sub> = V <sub>IL</sub>	0.9 – 4.5	0.9 – 4.5		0.2	V	
		I <sub>OL</sub> = 0.5 mA; V <sub>I</sub> = V <sub>IL</sub>	0.9	0.9		0.25 * V <sub>CCO</sub>		
		I <sub>OL</sub> = 2 mA; V <sub>I</sub> = V <sub>IL</sub>	1.4	1.4		0.35		
		I <sub>OL</sub> = 4 mA; V <sub>I</sub> = V <sub>IL</sub>	1.65	1.65		0.45		
		I <sub>OL</sub> = 8 mA; V <sub>I</sub> = V <sub>IL</sub>	2.3	2.3		0.55		
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>	3.0	3.0		0.7		
		I <sub>OL</sub> = 12 mA; V <sub>I</sub> = V <sub>IL</sub>	4.5	4.5		0.75		
I <sub>I</sub>	Input Leakage Current	V <sub>I</sub> = V <sub>CCA</sub> or GND	$\overline{nOE}$	0.9 – 4.5	0.9 – 4.5		±2.5	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V,	nA	0	0 – 4.5		±10.0	μA
			nB	0 – 4.5	0		±10.0	
I <sub>OZ</sub> <sup>(3)</sup>	3-State Output Leakage Current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = V <sub>CCO</sub> or GND, $\overline{nOE}$ = V <sub>IH</sub>	nA, nB	3.6	3.6		±12.5	μA
			nA	3.6	0		±12.5	
			nB	0	3.6		±12.5	
I <sub>CCA</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC1</sub> or GND; I <sub>O</sub> = 0		0.9	0.9		20	μA
				1.6	1.6		20	
				1.95	1.95		20	
				2.7	2.7		30	
				0	3.6		-40	
				3.6	0		40	
				3.6	3.6		40	
				0	4.5		-40	
				4.5	0		40	
	4.5	4.5		40				
I <sub>CCB</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC1</sub> or GND; I <sub>O</sub> = 0		0.9	0.9		20	μA
				1.6	1.6		20	
				1.95	1.95		20	
				2.7	2.7		30	
				0	3.6		-40	
				3.6	0		40	
				3.6	3.6		40	
				0	4.5		-40	
				4.5	0		40	
	4.5	4.5		40				

NOTE: Connect ground before applying supply voltage V<sub>CCA</sub> or V<sub>CCB</sub>. This device is designed with the feature that the power-up sequence of V<sub>CCA</sub> and V<sub>CCB</sub> will not damage the IC.

3. V<sub>CC1</sub> is the V<sub>CC</sub> associated with the input port.

4. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

5. For I/O ports, the parameter IOZ includes the input leakage current.

# NLA16T245

## AC ELECTRICAL CHARACTERISTICS – See Figure 3

Symbol	Parameter	From	To	-55°C to +115°C										Unit
				V <sub>CCB</sub> (V)										
				4.0 – 4.5		3.0 – 3.6		2.3 – 2.7		1.65 – 1.95		1.4 – 1.6		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	

### V<sub>CCA</sub> = 4.0 – 4.5 V

t <sub>PD</sub>	Propagation Delay	A	B	0.5	3.2	0.3	3.2	0.7	3.5	0.8	4.2	0.4	4	ns
		B	A	0.3	4.5	0.5	5.8	0.5	6	0.7	6.3	1.2	6.8	
t <sub>EN</sub>	Output Enable		A	0.2	9.5	1.0	7.7	0.9	8	1.0	9	0.8	8.5	ns
			B	0.8	4.5	1.2	4.8	1.4	6.7	1.8	7	1.6	7.5	
t <sub>DIS</sub>	Output Disable		A	0.8	5.6	1.0	5.6	1.1	5.6	1.1	5.7	1.2	5.7	ns
			B	1.2	6	1.2	6.1	1.1	6	2.6	9.2	2.3	9.6	
t <sub>OSK</sub>	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

### V<sub>CCA</sub> = 3.0 – 3.6 V

t <sub>PD</sub>	Propagation Delay	A	B	0.5	3.5	0.5	3.1	0.5	3.7	0.7	5.4	0.5	5.9	ns
		B	A	0.6	5.5	0.4	5.5	0.7	5.5	0.7	5.8	1.0	6.5	
t <sub>EN</sub>	Output Enable		A	0.8	10	1.0	8	1.3	8.0	1.4	9.2	1.3	8.7	ns
			B	1.0	5	1.9	4.9	2.0	5.4	1.9	6.7	0.8	7.4	
t <sub>DIS</sub>	Output Disable		A	1.5	6	1.5	5.4	1.2	5.8	1.6	5.2	1.4	5.4	ns
			B	1.7	6.4	1.5	6.1	1.1	5.8	1.7	8.5	1.2	8.8	
t <sub>OSK</sub>	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

### V<sub>CCA</sub> = 2.3 – 2.7 V

t <sub>PD</sub>	Propagation Delay	A	B	0.7	4	0.5	3.4	0.4	4.0	0.7	5.6	0.2	6.0	ns
		B	A	0.6	4.7	0.5	5.3	0.6	5.0	1.2	5.8	1.0	6.1	
t <sub>EN</sub>	Output Enable		A	0.9	12	2.0	9.0	1.7	7.0	1.6	7.9	1.6	8.0	ns
			B	0.7	5.7	1.5	5.3	2.2	6.1	2.2	7.0	1.2	7.8	
t <sub>DIS</sub>	Output Disable		A	2	6.8	1.6	6.2	0.7	6.5	1.5	6.0	2.0	6.5	ns
			B	1.2	6	1.4	6.0	1.0	5.6	1.7	8.2	0.9	9.0	
t <sub>OSK</sub>	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

### V<sub>CCA</sub> = 1.65 – 1.95 V

t <sub>PD</sub>	Propagation Delay	A	B	1.1	4.2	0.8	4.3	0.9	4.7	1.0	6.0	0.6	6.4	ns
		B	A	1.2	4.5	1.3	5.5	0.9	5.8	1.8	6.7	1.4	6.5	
t <sub>EN</sub>	Output Enable		A	2.2	9.7	2.0	8.5	2.2	8.9	2.1	9.5	2.5	10.0	ns
			B	0.5	8.2	2.7	8.1	2.7	8.1	2.7	8.3	1.8	9.0	
t <sub>DIS</sub>	Output Disable		A	2	9.3	1.8	8.0	1.5	8.0	2.5	8.8	2.1	8.6	ns
			B	1.8	6.2	2.0	6.1	1.0	5.5	2.5	8.3	2.1	8.8	
t <sub>OSK</sub>	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

### V<sub>CCA</sub> = 1.4 – 1.6 V

t <sub>PD</sub>	Propagation Delay	A	B	1.2	5	1.3	5.8	1.0	5.5	1.5	6.3	1.7	6.7	ns
		B	A	1	5.5	0.7	7.3	0.9	7.6	1.5	7.4	1.8	6.8	

# NLA16T245

## AC ELECTRICAL CHARACTERISTICS – See Figure 3

Symbol	Parameter	From	To	-55°C to +115°C										Unit
				V <sub>CCB</sub> (V)										
				4.0 – 4.5		3.0 – 3.6		2.3 – 2.7		1.65 – 1.95		1.4 – 1.6		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	

V<sub>CCA</sub> = 1.4 – 1.6 V

t <sub>EN</sub>	Output Enable		A	3	11.5	2.1	10.5	2.3	10.5	2.7	12.0	2.6	12.8	ns
			B	2	10	3.2	10.7	3.2	10.8	3.2	10.2	2.7	10.6	
t <sub>DIS</sub>	Output Disable		A	3	12	2.0	10.5	1.7	10.5	2.5	9.5	2.1	9.7	ns
			B	1.2	6	1.3	6.4	1.1	6.5	2.5	8.5	2.1	8.8	
t <sub>OSK</sub>	Output to Output Skew				0.15		0.15		0.15		0.15		0.15	ns

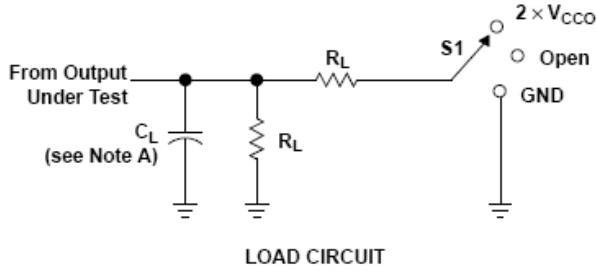
## CAPACITANCES

Symbol	Parameter	Output State	Test Conditions	Typ (Note 6)	Unit
C <sub>IN</sub>	Control Pin Input Capacitance		V <sub>I</sub> = 3.3 V or GND	3.5	pF
C <sub>I/O</sub>	I/O Pin Input Capacitance		V <sub>O</sub> = 3.3 V or GND	5.0	pF
C <sub>PD(A)</sub> (Note 7)	Power Dissipation Capacitance per	Enabled	C <sub>L</sub> = 0 pF, f = 10 MHz	14.0	pF
	Transceiver, A–Port Input, B–Port Output	Disabled		7.0	
	Power Dissipation Capacitance per	Enabled		20.0	
	Transceiver, B–Port Input, A–Port Output	Disabled		7.0	
C <sub>PD(B)</sub> (Note 7)	Power Dissipation Capacitance per	Enabled	C <sub>L</sub> = 0 pF, f = 10 MHz	14.0	pF
	Transceiver, A–Port Input, B–Port Output	Disabled		7.0	
	Power Dissipation Capacitance per	Enabled		20.0	
	Transceiver, B–Port Input, A–Port Output	Disabled		7.0	

6. Typical values are at V<sub>CCA</sub> = V<sub>CCB</sub> = 3.3 V, T<sub>A</sub> = +25°C.

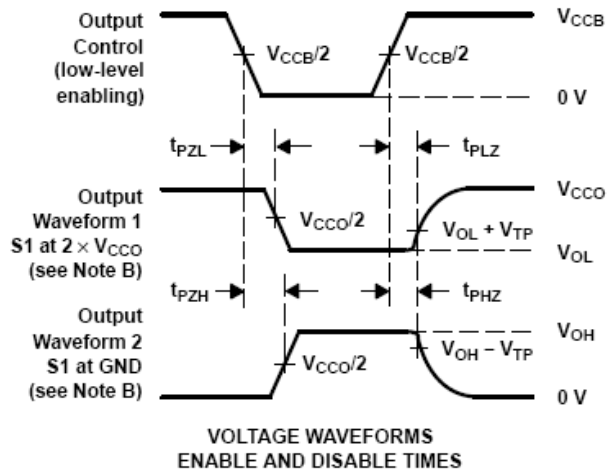
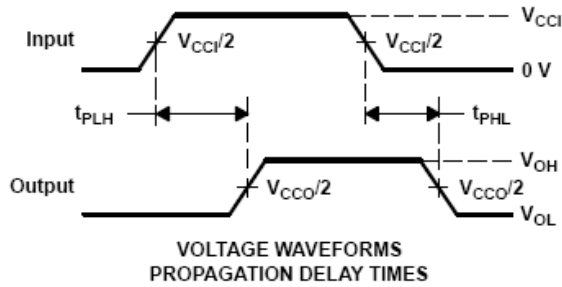
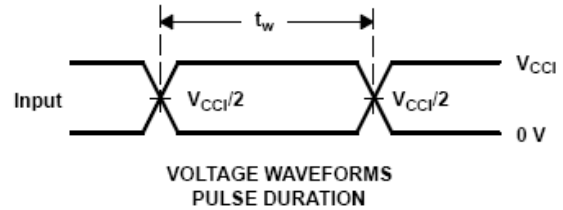
7. C<sub>PD</sub> is defined as the value of the IC's equivalent capacitance from which the operating current can be calculated from:  
I<sub>CC(operating)</sub> ≈ C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> × N<sub>SW</sub> where I<sub>CC</sub> = I<sub>CCA</sub> + I<sub>CCB</sub> and N<sub>SW</sub> = total number of outputs switching.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.5\text{ V} \pm 0.1\text{ V}$	15 pF	2 k $\Omega$	0.1 V
$1.8\text{ V} \pm 0.15\text{ V}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	30 pF	500 $\Omega$	0.3 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H.  $V_{CC1}$  is the  $V_{CC}$  associated with the input port.
  - I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

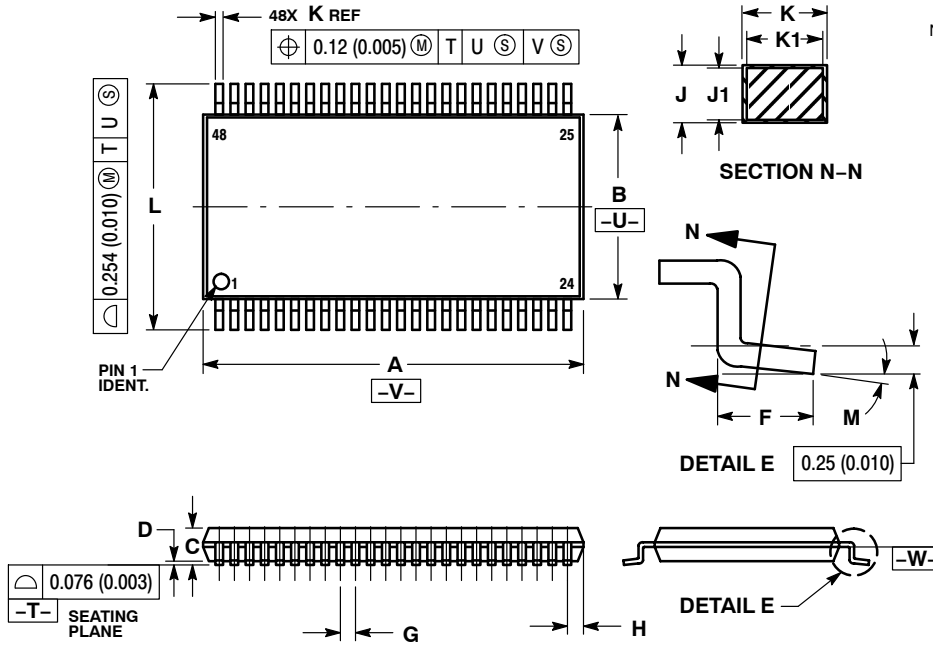
Figure 3. Load Circuit and Voltage Waveforms



# NLA16T245

## PACKAGE DIMENSIONS

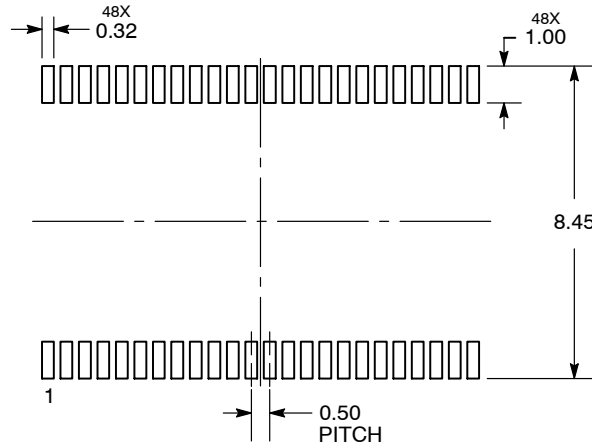
TSSOP-48  
CASE 1201  
ISSUE B



### NOTES:


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.


## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative